

IN THE CLAIMS:

Please Cancel Claims 1-12 and 25-28

Please add the following new claims 29-39 for examination:

29. (Newly Submitted) A method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device, said method comprising the steps of:

providing a substrate;

thereafter configuring said substrate to comprise a wiring bond pad to comprise a single metal layer, wherein said single metal layer does not share said single metal layer with any other material;

thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad to comprise a single metal layer;

thereafter locating a buffer and bonding layer immediately above said single metal layer;

thereafter locating said single metal layer above a plurality of intermetal dielectric layers; and

thereafter locating said at least one integrated circuit device below said plurality of intermetal dielectric layers, wherein said single metal layer comprises a metal-8 layer.

30. (Newly Submitted) The method of claim 29 wherein said plurality of intermetal dielectric layers comprises at least IMD-1 to IMD-7 layers.

31. (Newly Submitted) The method of claim 29 wherein said metal-8 layer comprises a copper layer.

32. A method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device, said method comprising the steps of:

providing a substrate;

thereafter configuring said substrate to comprise a wiring bond pad to comprise a single metal layer, wherein said single metal layer does not share said single metal layer with any other material;

thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad to comprise a single metal layer;

thereafter locating a buffer and bonding layer immediately above said single metal layer;

thereafter locating said single metal layer above a plurality of intermetal dielectric layers, wherein said plurality of intermetal dielectric layers comprises at least IMD-1 to IMD-7 layers; and

thereafter locating said at least one integrated circuit device below said plurality of intermetal dielectric layers, wherein said single metal layer comprises a metal-8 layer of copper;

thereafter forming a layer of aluminum film above said single metal layer, wherein said layer of aluminum film above said single metal layer comprises a buffer and bonding layer.

33. (Newly submitted) The method of claim 32 wherein said layer of aluminum film formed above said single metal layer comprises a layer having a thickness in a range of and including 10KÅ to 20KÅ.

33. (Newly Submitted) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately 10KÅ.

34. (Newly Submitted) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately 12KÅ.

35. (Newly Submitted) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately $14\text{K}\text{\AA}$.

36. (Newly Submitted) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately $16\text{K}\text{\AA}$.

B. Amad
37. (Newly Submitted) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately $18\text{K}\text{\AA}$.

38. (Newly Submitted) A method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device, said method comprising the steps of:

providing a substrate;

configuring on said substrate, a wiring bond pad comprising a single metal layer, wherein said single metal layer comprises a copper layer;

thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad as a single metal layer, wherein said single metal layer comprises a single metal layer isolated from other layers and metals of said wiring bond pad;

thereafter locating said wiring bond pad above a plurality of intermetal dielectric layers, wherein said plurality of intermetal dielectric layers comprises at least IMD-1 to IMD-7 layers; and

thereafter forming a layer of aluminum film above said wiring bond pad, such that said layer of aluminum film comprises a thickness of approximately $15\text{K}\text{\AA}$, wherein said layer of aluminum film above said wiring bond pad comprises a buffer and bonding layer.

39. (Newly Submitted) The method of claim 38 wherein said layer of aluminum film above said wiring bond pad comprises a bonding layer.